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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HUNG THANH	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,253	CHAO, YUAN-JEN	
	Examiner	Art Unit	
	HUNG T. NGUYEN	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US 5903239) in view of Stopperan (US 5719749)

Regard claim 1: Takahashi et al. discloses in figures 2-3 a multi-chip integrated module, comprising: a transparent substrate (1a, see column 4 on line 38-41), which has a circuit layer formed on one surface of the transparent substrate (1a, see column 4 on line 38-41), wherein the circuit layer formed on the surface of the transparent substrate (1a, see column 4 on line 38-41) comprises a circuit (combination of chips 52, 54 and interconnection terminals) for electrical inter-connection and a plurality of electrical pads (4); at least two chips (52, 54), which are respectively mounted on the transparent substrate (1a, see column 4 on line 38-41) by way of a flip-chip bonding (see abstract and further), wherein the chips (52, 54) and the circuit (combination of chips 52, 54 and interconnection terminals) for electrical interconnection construct a circuit system.

Takahashi et al. does not disclose a circuit substrate, which attaches to the transparent substrate, and at least comprises a circuit layer of the circuit substrate, wherein the

electrical pads of the transparent substrate electrically connect to the circuit layer of the circuit substrate.

Stopperan discloses in figure 1, a circuit substrate (40) which attaches to the transparent substrate, and at least comprises a circuit layer (see overlay 40) of the circuit substrate (40), wherein the electrical pads (36, 68) of the transparent substrate electrically connect to the circuit layer of the circuit substrate (40).

Takahashi et al. and Stopperan are analogous art because they are from the same field of endeavor to make circuit board.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to make a circuit substrate attached to transparent substrate of Takahashi, as taught by Stopperan.

The motivation to do is the benefit of reducing cost and better heat dissipation because the circuit is less minimized. Also, added layer help increase circuit capacity.

Regard claim 2, 15: Takahashi discloses the multi-chip integrated wherein the transparent substrate is a glass substrate (1a, see column 4 on line 38-41).

Regard claim 3: Takahashi discloses in figures 1-4 the multi-chip integrated module wherein a plurality of bumps (6a, 6b) are formed on the electrical pads (4) of the transparent substrate (explain above) electrically connecting the electrical substrate (explain above), respectively, for pads and the circuit layer of the circuit.

Regard claim 4: Takahashi discloses in figures 1-4 the multi-chip integrated wherein a plurality of bumps (explain above) are formed on a part of the circuit (see figure 1-4) for

electrical inter-connection, and the chips (explain above) electrically connect to the bumps by way of a flip-chip bonding (explain above).

Regard claim 5, 16: Takahashi discloses the multi-chip integrated module wherein the bumps are solder bumps (see column 2, line 24).

Regard claim 6, 17: Takahashi discloses the multi-chip integrated module wherein the bumps are gold bumps (see column 2, line 24).

Regard claim 7, 18: Takahashi discloses all elements the multi-chip integrated module as described above with respect to claim 1 except, Takahashi does not disclose the bumps are copper bumps.

It is old and well known for one ordinary in the art to make bump by copper because it provides good conduction and cheap.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to make the bumps of Takahashi copper to reduce the cost.

Regard claim 8: Takahashi discloses the multi-chip integrated module wherein the circuit substrate (explain above) has a hollow portion (see abstract and column 1, line 33-67), and when the circuit substrate (explain above) attaches to the transparent substrate (explain above), the chips (explain above) are positioned in the hollow portion (explain above) of the circuit substrate (explain above).

Regard claim 9: Takahashi discloses all the elements of the multi-chip integrated module as described above with respect to claim 1 except, Takahashi does not disclose a heat dissipation element is formed on the backside of at least one of the chips.

Making the heat sink depends on the applications. Sometimes heat sinks are on the back of the IC's and sometimes they are separated.

Heat skinks are old and well known and help to cool the device so it function properly.

Therefore, it would have been obvious to one of ordinary skill at the time of the invention to combine a heat sink on the chips of Takahashi for the benefit of reducing heat and also preventing to damage to the IC's.

Regard claim 10: Takahashi discloses the multi-chip integrated module wherein the circuit substrate is a printed circuit substrate (FPC, see column 3, line 30-43).

Regard claim 11,19: Takahashi discloses the multi-chip integrated module further comprising: a passive component (see column 7, line 49-54) which is formed on the transparent substrate (explain above) and electrically connects to the circuit (explain above) for electrical inter-connection on the transparent substrate (explain above).

Regard claim 12, 20: Takahashi discloses the multi-chip integrated module of claim 1, further comprising: an active component (see column 7, line 49-54) which is formed on the transparent substrate (explain above) and electrically connects to the circuit (explain above) for electrical inter-connection on the transparent substrate (explain above).

Regard claim 13: Takahashi discloses in figure 1-4 a multi-chip integrated module, comprising: a transparent substrate (explain in claim 1), which has a circuit layer formed on one surface of the transparent substrate (explain in claim 1), wherein the circuit layer formed on the surface of the transparent substrate (explain in claim 1) comprises a circuit (explain in claim 1) for electrical inter-connection, and a plurality of bumps (explain in claim 3) are formed on a part of the circuit (explain above) for electrical inter-

connection; and at least two chips (explain in claim 1), which electrically connect to the bumps (explain in claim 3) of the circuit (explain above) for electrical inter-connection by way of a flip-chip bonding (explain in claim 3), wherein the chips and the circuit for electrical inter-connection construct a circuit system.

Regard claim 14: Takahashi discloses in figure 1-9 the multi-chip integrated module wherein the circuit layer of the transparent substrate (explain in claim 1) further comprises a plurality of electrical pads (see figures 1-9) for electrical external-connection, and a plurality of bumps (explain above) are formed on the electrical pads (explain above), respectively.

Relevant Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Imasu et al. (US 6208525) teaches the Process For Mounting Electronic Devices, Kim (US 6310299) teaches the Glass Connector And Fabricating, Tagusa et al. (US 5668700) teaches the Panel Assembly Structure, Bertin et al. (US 6255899) teaches the Method and Apparatus for Increasing Interchip and Mehta (US 4758459) teaches the Molded Circuit Board.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUNG T. NGUYEN whose telephone number is 571-272-5983. The examiner can normally be reached on 8:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KAMMIE CUNEO can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

HN

Hung Thanh Nguyen

August 2, 2005

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